

1. A method of using dual damascene comprising:
providing a substrate having an insulator layer
deposited thereon;

depositing a low dielectric constant material, as
5 an intermetal dielectric (IMD) layer, over said
substrate;

depositing a multilayer interface layer over the
intermetal dielectric layer (IMD) comprised of a bottom
hard film layer and a top soft film layer;

10 depositing a dielectric anti-reflective coating
(DARC) over the multilayer interface layer;

patterning and forming dual damascene trench/via
openings in said intermetal dielectric (IMD) layer,
along with the exposed dielectric anti-reflective
15 coating (DARC) and the exposed multilayer interface;

removing the patterning and masking material;

depositing a metal diffusion barrier layer and a
copper seed layer into the dual damascene trench/via
openings of the intermetal dielectric (IMD) layer and
20 over said substrate and over the dielectric
anti-reflective coating (DARC);

depositing a copper metal layer over said copper
seed layer, filling the dual damascene trench/via;

polishing off the excess materials, thereby
25 planarizing the surface to form conductive
interconnects and contacts to the underlying substrate.

2. The method of claim 1, wherein said low dielectric constant material, as an intermetal dielectric layer (IMD) or layers, and in general, the insulating layers, are selected from the group consisting of "Silk C.H.O. (polymer based)", FLARE or low-K polymer, silicon dioxide or silicon oxide, and/or silicon nitride, deposited by chemical vapor deposition (CVD), in the thickness range from approximately 1,000 to 5,000 Angstroms.
3. The method of claim 1, wherein said multilayer interface layer comprised of said bottom hard film layer is selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide, deposited by chemical vapor deposition (CVD), in the thickness range from approximately 100 to 500 Angstroms.
4. The method of claim 1, wherein said multilayer interface layer comprised of said top soft film layer is selected from the group consisting of silicon oxide, plasma enhanced (PE) oxide, plasma enhanced (PE) TEOS, tetraethylorthosilicate, low dielectric constant materials, FLARE or polymer in the thickness range from approximately 100 to 500 Angstroms.

5. The method of claim 1, wherein said multilayer interface layer is comprised of a bottom hard film layer and a top soft film layer.

5 6. The method of claim 1, wherein said multilayer interface layer is comprised of a bottom soft film layer and a top hard film layer.

7. The method of claim 1, wherein said dielectric anti-reflective coating (DARC) is selected from the group consisting of silicon oxynitride, silicon carbide, and is deposited by chemical vapor deposition (CVD), over said multilayer interface layer, in the thickness range from approximately 300 to 600 Angstroms.

15 8. The method of claim 1, wherein the hard film layer polishing properties, selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide, have a slower polishing removal rate than that of copper.

9. The method of claim 1, wherein the soft film layer polishing properties, selected from the group consisting of silicon oxide, plasma enhanced (PE) oxide, plasma enhanced (PE) TEOS, tetraethylorthosilicate, low

dielectric constant materials, FLARE or polymer, have a faster polishing removal rate than that of copper.

10. The method of claim 1, wherein the multilevel
5 interface layer polishing properties comprised of both a hard layer selected from the group consisting of silicon nitride, silicon oxynitride, and a soft layer selected from the group consisting of silicon oxide, plasma enhanced (PE) oxide, plasma enhanced (PE) TEOS,
10 tetraethylorthosilicate, low dielectric constant materials, FLARE or low-K polymer, act in combination during polishing to form planarized copper.

11. The method of claim 1, wherein the trenches or
15 channels for metal interconnects and via hole contact openings contain a barrier, diffusion barrier liner or diffusion barrier layer, which also aids adhesion, deposited by sputtering (PVD), liner barrier material selected from the group consisting of Ta, TaN and, in a
20 thickness range from about 100 to 4,000 Angstroms.

12. The method of claim 1, wherein the damascene trench or channel interconnects and via hole contacts can be comprised of a copper seed layer liner, for
25 interconnects and contact vias, deposited by sputtering

(PVD), seed type materials comprising of thin Cu, thickness from about 1,000 to 10,000 Angstroms.

13. The method of claim 1, wherein said copper
5 metal layer is selected from the group consisting of Cu, AlCu alloys and AlCuSi alloys.

14. The method of claim 1, wherein the damascene
openings is filled with a layer of copper, inlaid
10 conducting material layer, forming conducting interconnect lines and contact vias for interconnects and contact vias, and is comprised of copper deposited by an electrochemical deposition (ECD), the Cu approximate thickness from 4,000 to 10,000 Angstroms.

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15. The method of claim 1, wherein damascene and dual damascene patterned openings, for subsequent inlaid metal, are formed by the following methods, selected from the group consisting of reactive ion etching (RIE),
20 milling, ion milling, wet etching, or a combination thereof.

16. The method of claim 1, wherein the levels of conducting metal copper layers are planarized by
25 removing excess conducting material to form inlaid dual damascene conducting metal interconnects, in trench and

via openings, and this process includes planarization by the following methods, selected from the group consisting of planarization by chemical mechanical polish (CMP), milling, ion milling, and/or etching, or a
5 combination thereof.

17. The method of claim 1, wherein one of the final processing steps is the forming by damascene and chemical mechanical polishing (CMP) the inlaid copper
10 metal layer, by removing the excess copper metal layers, the excess barrier layer, and the multilevel interface layer including the dielectric anti-reflective coating (DARC), thus planarizing the surface by chemical mechanical polishing (CMP), forming smooth surface
15 inlaid copper, which remains in the open regions.

18. A method of using dual damascene technique to a conductive interconnect wiring and contact via to a semiconductor diffusion in the fabrication of MOSFET
20 devices comprising:

providing a semiconductor substrate having a semiconductor diffusion region therein;

depositing a low dielectric constant material, as an intermetal dielectric (IMD) layer, over said
25 semiconductor substrate and the semiconductor diffusion region;

depositing a multilayer interface layer over the intermetal dielectric layer (IMD) comprised of a bottom hard film layer and a top soft film layer;

depositing a dielectric anti-reflective coating
5 (DARC) over the multilayer interface layer;

patterning and etching dual damascene trench/via openings in said intermetal dielectric (IMD) layer, along with the exposed dielectric anti-reflective coating (DARC) and the exposed multilayer interface
10 layer;

removing the patterning and masking material;

depositing a metal diffusion barrier layer and a copper seed layer into the dual damascene trench/via openings of the intermetal dielectric (IMD) layer and
15 over said semiconductor diffusion region and over the dielectric anti-reflective coating (DARC);

depositing a copper metal layer by electrochemical deposition (ECD) over said copper seed layer, filling the dual damascene trench/via openings;

20 polishing off the excess copper metal, the dielectric anti-reflective coating (DARC) layer, the multilayer interface layer, the excess copper seed layer and the excess barrier layer outside of the thrench/via openings, thereby planarizing the surface to form a
25 conductive interconnect wiring and contact via to the underlying semiconductor diffusion region.

19. The method of claim 18, wherein said contact is made to a semiconductor diffusion region on a semiconductor substrate.

5 20. The method of claim 18, wherein the dual damascene process is compatible with MOSFET CMOS processing, devices and circuits, for both logic and memory applications.

10 21. The method of claim 18, wherein said low dielectric constant material, as an intermetal dielectric layer (IMD) or layers, and in general, the insulating layers, are selected from the group consisting of "Silk C.H.O. (polymer based)", FLARE or
15 polymer, silicon dioxide or silicon oxide, and/or silicon nitride, deposited by chemical vapor deposition (CVD), in the thickness range from approximately 1,000 to 5,000 Angstroms.

20 22. The method of claim 18, wherein said multilayer interface layer comprised of said bottom hard film layer is selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide, deposited by chemical vapor deposition (CVD), in the
25 thickness range from approximately 100 to 500 Angstroms.

23. The method of claim 18, wherein said
multilayer interface layer comprised of said top soft
film layer is selected from the group consisting of
silicon oxide, plasma enhanced (PE) oxide, plasma
5 enhanced (PE) TEOS, tetraethylorthosilicate, low
dielectric constant polymer materials, in the thickness
range from approximately 100 to 500 Angstroms.

24. The method of claim 18, wherein said
10 multilayer interface layer is comprised of a bottom hard
film layer and a top soft film layer.

25. The method of claim 18, wherein said
multilayer interface layer is comprised of a bottom soft
15 film layer and a top hard film layer.

26. The method of claim 18, wherein said
dielectric anti-reflective coating (DARC) is selected
from the group consisting of silicon oxynitride, and is
20 deposited by chemical vapor deposition (CVD), over said
multilayer interface layer, in the thickness range from
approximately 300 to 600 Angstroms.

27. The method of claim 18, wherein the hard film
25 layer polishing properties, selected from the group
consisting of silicon nitride, silicon oxynitride,

silicon carbide, have a slower polishing removal rate than that of copper.

28. The method of claim 18, wherein the soft film
5 layer polishing properties, selected from the group
consisting of silicon oxide, plasma enhanced (PE) oxide,
plasma enhanced (PE) TEOS, tetraethylorthosilicate, low
dielectric constant polymer materials, have a faster
polishing removal rate than that of copper.

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29. The method of claim 18, wherein the multilevel
interface layer polishing properties comprised of both a
hard layer selected from the group consisting of silicon
nitride, silicon oxynitride, silicon carbide and a soft
15 layer selected from the group consisting of silicon
oxide, plasma enhanced (PE) oxide, plasma enhanced (PE)
TEOS, tetraethylorthosilicate, low dielectric constant
polymer materials, act in combination during polishing
to form planarized copper.

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30. The method of claim 18, wherein the trenches
or channels for metal interconnects and via hole contact
openings contain a barrier, diffusion barrier liner or
diffusion barrier layer, which also aids adhesion,
25 deposited by sputtering (PVD), liner barrier material

selected from the group consisting of Ta, TaN and, in a thickness range from about 100 to 4,000 Angstroms.

31. The method of claim 18, wherein the damascene
5 trench or channel interconnects and via hole contacts can be comprised of a copper seed layer liner, for interconnects and contact vias, deposited by sputtering (PVD), seed type materials comprising of thin Cu, thickness from about 1,000 to 10,000 Angstroms.

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32. The method of claim 18, wherein the conductor wiring or conducting material consists of the following and is selected from the group consisting of Cu, AlCu alloys, and AlCuSi alloys.

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33. The method of claim 18, wherein said copper metal layer is selected from the group consisting of Cu, AlCu alloys and AlCuSi alloys.

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34. The method of claim 18, wherein the damascene openings is filled with a layer of copper, inlaid conducting material layer, forming conducting interconnect lines and contact vias for interconnects and contact vias, and is comprised of copper deposited
25 by an electrochemical deposition (ECD), the Cu approximate thickness from 4,000 to 10,000 Angstroms.

35. The method of claim 18, wherein damascene and dual damascene patterned openings, for subsequent inlaid metal, are formed by the following methods, selected from the group consisting of reactive ion etching (RIE),
5 milling, ion milling, wet etching, or a combination thereof.

36. The method of claim 18, wherein the levels of conducting metal copper layers are planarized by
10 removing excess conducting material to form inlaid dual damascene conducting metal interconnects, in trench and via openings, and this process includes planarization by the following methods, selected from the group consisting of planarization by chemical mechanical
15 polish (CMP), milling, ion milling, and/or etching, or a combination thereof.

37. The method of claim 18, wherein one of the final processing steps is the forming by damascene and
20 chemical mechanical polishing (CMP) the inlaid copper metal layer, by removing the excess copper metal layers, the excess barrier layer, and the multilevel interface layer including the dielectric anti-reflective coating (DARC), thus planarizing the surface by chemical
25 mechanical polishing (CMP), forming smooth surface inlaid copper, which remains in the open regions.

38. A method of using dual damascene technique to form a conductive interconnect wiring and contact via to first level conductor wiring comprising:

providing a substrate having a layer of dielectric;

5 providing a first level conductor wiring surrounded by barrier material within the said layer of dielectric;

depositing a low dielectric constant material, as an intermetal dielectric (IMD) layer, over said first level conductor wiring;

10 depositing a multilayer interface layer over the intermetal dielectric layer (IMD) comprised of a bottom hard film layer and a top soft film layer;

depositing a dielectric anti-reflective coating (DARC) over the multilayer interface layer;

15 patterning and etching dual damascene trench/via openings in said intermetal dielectric (IMD) layer, along with the exposed dielectric anti-reflective coating (DARC) and the exposed multilayer interface layer;

20 removing the patterning and masking material;

depositing a metal diffusion barrier layer and a copper seed layer into the dual damascene trench/via openings of the intermetal dielectric (IMD) layer and over said first level of conductor wiring and over the dielectric anti-reflective coating (DARC);

25 depositing a copper metal layer by electrochemical

deposition (ECD) over said copper seed layer, filling the dual damascene trench/via openings;

polishing off the excess copper metal, the dielectric anti-reflective coating (DARC) layer, the
5 multilayer interface layer, the excess copper seed layer and the excess barrier layer outside of the thrench/via openings, thereby planarizing the surface to form inlaid copper interconnect wiring and contact vias to first level conductor wiring.

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39. The method of claim 38, wherein said substrate is semiconductor substrate or an IC module.

40. The method of claim 38, wherein the dual
15 damascene process is compatible with MOSFET CMOS processing, devices and circuits, for both logic and memory applications.

41. The method of claim 38, wherein said low
20 dielectric constant material, as an intermetal dielectric layer (IMD) or layers, and in general, the insulating layers, are selected from the group consisting of "Silk C.H.O. (polymer based)", low-k polymer materials, silicon dioxide or silicon oxide,
25 and/or silicon nitride, deposited by chemical vapor

deposition (CVD), in the thickness range from approximately 1,000 to 5,000 Angstroms.

42. The method of claim 38, wherein said
5 multilayer interface layer comprised of said bottom hard film layer is selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide, deposited by chemical vapor deposition (CVD), in the thickness range from approximately 100 to 500 Angstroms.

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43. The method of claim 38, wherein said
multilayer interface layer comprised of said top soft film layer is selected from the group consisting of silicon oxide, plasma enhanced (PE) oxide, plasma
15 enhanced (PE) TEOS, tetraethylorthosilicate, low dielectric constant polymer materials, in the thickness range from approximately 100 to 500 Angstroms.

44. The method of claim 38, wherein said
20 multilayer interface layer is comprised of a bottom hard film layer and a top soft film layer.

45. The method of claim 38, wherein said
multilayer interface layer is comprised of a bottom soft
25 film layer and a top hard film layer.

46. The method of claim 38, wherein said dielectric anti-reflective coating (DARC) is selected from the group consisting of silicon oxynitride, and is deposited by chemical vapor deposition (CVD), over said
 5 multilayer interface layer, in the thickness range from approximately 300 to 600 Angstroms.

47. The method of claim 38, wherein the hard film layer polishing properties, selected from the group
 10 consisting of silicon nitride, silicon oxynitride, silicon carbide, have a slower polishing removal rate than that of copper.

48. The method of claim 38, wherein the soft film
 15 layer polishing properties, selected from the group consisting of silicon oxide, plasma enhanced (PE) oxide, plasma enhanced (PE) TEOS, tetraethylorthosilicate, low dielectric constant polymer materials, have a faster polishing removal rate than that of copper.

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49. The method of claim 38, wherein the multilevel interface layer polishing properties comprised of both a hard layer selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide, and a soft
 25 layer selected from the group consisting of silicon oxide, plasma enhanced (PE) oxide, plasma enhanced (PE)

TEOS, tetraethylorthosilicate, low dielectric constant polymer materials, act in combination during polishing to form planarized copper.

5 50. The method of claim 38, wherein the trenches
or channels for metal interconnects and via hole contact
openings contain a barrier, diffusion barrier liner or
diffusion barrier layer, which also aids adhesion,
deposited by sputtering (PVD), liner barrier material
10 selected from the group consisting of Ta, TaN and, in a
thickness range from about 100 to 4,000 Angstroms.

 51. The method of claim 38, wherein the damascene
trench or channel interconnects and via hole contacts
15 can be comprised of a copper seed layer liner, for
interconnects and contact vias, deposited by sputtering
(PVD), seed type materials comprising of thin Cu,
thickness from about 1,000 to 10,000 Angstroms.

20 52. The method of claim 38, wherein said first
level conductor wiring or conducting material consists
of the following and is selected from the group
consisting of Cu, AlCu alloys, AlCuSi alloys and W.

53. The method of claim 38, wherein said copper metal layer is selected from the group consisting of Cu, AlCu alloys and AlCuSi alloys.

5 54. The method of claim 38, wherein the damascene openings is filled with a layer of copper, inlaid conducting material layer, forming conducting interconnect lines and contact vias for interconnects and contact vias, and is comprised of copper deposited
10 by an electrochemical deposition (ECD), the Cu approximate thickness from 4,000 to 10,000 Angstroms.

55. The method of claim 38, wherein damascene and dual damascene patterned openings, for subsequent inlaid
15 metal, are formed by the following methods, selected from the group consisting of reactive ion etching (RIE), milling, ion milling, wet etching, or a combination thereof.

20 56. The method of claim 38, wherein the levels of conducting metal copper layers are planarized by removing excess conducting material to form inlaid dual damascene conducting metal interconnects, in trench and via openings, and this process includes planarization by
25 the following methods, selected from the group consisting of planarization by chemical mechanical

polish (CMP), milling, ion milling, and/or etching, or a combination thereof.

57. The method of claim 38, wherein one of the
5 final processing steps is the forming by damascene and
chemical mechanical polishing (CMP) the inlaid copper
metal layer, by removing the excess copper metal layers,
the excess barrier layer, and the multilevel interface
layer including the dielectric anti-reflective coating
10 (DARC), thus planarizing the surface by chemical
mechanical polishing (CMP), forming smooth surface
inlaid copper, which remains in the open regions.